WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a first silicon film over a semiconductor substrate and forming a first dielectric film over the first silicon film;

(b) patterning the first dielectric film and the first silicon film thereby forming, in the first region within the main surface of the semiconductor substrate, a lower electrode of a capacitor element comprising the first silicon film and a capacitor insulation film of the capacitor element comprising the first dielectric film and forming a resistor element comprising the first silicon film in the second region within the main surface of the semiconductor substrate;

(c) forming a first conductive film over the semiconductor substrate in the presence of the lower electrode and the capacitor insulation film of the capacitor element and the resistor element; and

(d) patterning the first conductive film thereby forming an upper electrode of the capacitor element comprising the first conductive film over the capacitor insulation film and forming a gate electrode of a power MISFET comprising the first conductive film in the third region over the main

surface of the semiconductor substrate.

2. A manufacturing method according to claim 1, wherein the step (a) includes:

(a1) oxidizing the surface of the first silicon film to form a first silicon oxide film;

(a2) forming a first silicon nitride film over the first silicon oxide film;

(a3) oxidizing the surface of the first silicon nitride film to form a second silicon oxide film; and

(a4) forming a third silicon oxide film over the second silicon oxide film to form the first dielectric film comprising the first silicon oxide film, the first silicon nitride film, the second silicon oxide film, and the third silicon oxide film.

3. A manufacturing method according to claim 1,

wherein the first conductive film is a stacked film formed by stacking a second silicon film and a refractory metal silicide film from the lower layer, or a stacked film formed by stacking the second silicon film, a barrier metal film and a refractory metal film from the lower layer.

4. A manufacturing method according to claim 1, comprising the steps of:

(e) forming a semiconductor chip of a planar rectangular shape having the power MISFET; and

(f) wire bonding the semiconductor chip to a mounting substrate by a first wire electrically connecting with the gate of the power MISFET and a second wire electrically connecting with the drain of the power MISFET,

wherein the power MISFET are arranged at four corners of the semiconductor chip, and the first wire and the second wire are arranged in the direction where they are in perpendicular to each other on a plane.

5. A manufacturing method according to claim 1,

wherein the capacitor element and the resistor element form an analog circuit.

6. A manufacturing method of a semiconductor device according to claim 5,

wherein the power MISFET forms a first circuit for processing signals in a first frequency band and a second circuit for processing signals in a second frequency band different from the first frequency band, and the analog circuit selects the first circuit or the second circuit.

7. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a first silicon film over a semiconductor substrate and forming a first dielectric film over the first silicon film;

(b) patterning the first dielectric film and the first silicon film thereby forming, in the first region within the main surface of the semiconductor substrate, a lower electrode of a capacitor element comprising the first silicon film and a capacitor insulation film of the capacitor element comprising the first dielectric film;

(c) forming a first conductive film over the semiconductor substrate in the presence of the lower electrode and the capacitor insulation film of the capacitor element;

(d) patterning the first conductive film thereby forming the upper electrode of the capacitor element comprising the first conductive film over the first portion of the lower electrode;

(e) forming a second dielectric film over the semiconductor substrate in the presence of the lower electrode, the capacitor insulation film and the upper electrode of the capacitor element;

(f) etching the second dielectric film and the capacitor insulation film using the upper electrode as an etching stopper thereby forming a first hole reaching the upper electrode and a second hole reaching a second portion of the lower electrode excepting for the first portion;

(g) forming plugs in the first hole and in the second hole;

(h) forming a second conductive film over the second dielectric film in the presence of the plugs; and

(i) patterning the second conductive film thereby forming a first wiring comprising the second conductive film and electrically connecting with the upper electrode and a second wirings comprising the second conductive film and electrically connecting with the lower electrode.

8. A manufacturing method according to claim 7,

wherein the first conductive film is a stacked film formed by stacking a second silicon film and a refractory metal silicide film from the lower layer, or a stacked film formed by stacking the second silicon film, a barrier metal film and a refractory metal film from the lower layer.

9. A manufacturing method according to claim 7, wherein the step (a) includes:

(a1) oxidizing the surface of the first silicon film to form a first silicon oxide film;

(a2) forming a first silicon nitride film over the first silicon oxide film;

(a3) oxidizing the surface of the first silicon nitride film to form a second silicon oxide film; and

(a4) forming a third silicon oxide film over the second

silicon oxide film to form the first dielectric film comprising the first silicon oxide film, the first silicon nitride film, the second silicon oxide film and the third silicon oxide film.

10. A manufacturing method according to claim 9, wherein the step (d) is conducted by etching using the first silicon nitride film as an etching stopper.

11. A manufacturing method according to claim 7,

wherein the step (b) includes a step of forming a resistor element comprising the first silicon film in the second region within the main surface of the semiconductor substrate, and the step (d) includes a step of forming a gate electrode of a power MISFET comprising the first conductive film in the third region over the main surface of the semiconductor substrate.

12. A manufacturing method according to claim 11, comprising the steps of:

(j) forming a semiconductor chip of a planar rectangular shape having the power MISFET; and

(k) wire bonding the semiconductor chip to a mounting substrate by a first wire electrically connecting with the gate of the power MISFET and a second wire electrically

connecting with the drain of the power MISFET,

wherein the power MISFET are arranged at four corners of the semiconductor chip, and the first wire and the second wire are arranged in the direction where they are in perpendicular to each other on a plane.

13. A manufacturing method according to claim 11,

wherein the capacitor element and the resistor element form an analog circuit.

14. A manufacturing method according to claim 13,

wherein the power MISFET forms a first circuit for processing signals in a first frequency band and a second circuit for processing signals in a second frequency band different from the first frequency band, and the analog circuit selects the first circuit or the second circuit.

15. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a first silicon film over a semiconductor substrate and forming a first dielectric film over the first silicon film;

(b) patterning the first dielectric film and the first silicon film thereby forming, in the first region within the main surface of the semiconductor substrate, a lower

electrode of a capacitor element comprising the first silicon film and a capacitor insulation film of the capacitor element comprising the first dielectric film, and forming a resistor element comprising the first silicon film in the second region within the main surface of the semiconductor substrate;

(c) forming a first conductive film over the semiconductor substrate in the presence of the lower electrode and the capacitor insulation film of the capacitor element, and the resistor element;

(d) patterning the first conductive film, thereby forming the upper electrode of the capacitor element comprising the first conductive film over the capacitor insulation film, forming the gate electrode of a first conduction type power MISFET comprising the first conductive film in the third region over the main surface of the semiconductor substrate, forming the gate electrode of the first conduction type first MISFET comprising the first conductive film in the fourth region over the main surface of the semiconductor substrate, and forming the gate electrode of a second conduction type second MISFET comprising the first conductive film in the fifth region over the main surface of the semiconductor substrate;

(e) introducing second conduction type impurities into a region for preventing the short channel effect of the power

MISFET; and

(f) introducing second conduction type impurities into a region for preventing the short channel effect of the first MISFET before the step(e) or after the step (e),

wherein the gate length of the gate electrode of the power MISFET is formed smaller than the gate length of the gate electrode of the second MISFET.

16. A manufacturing method of a semiconductor device according to claim 15, wherein the step (a) includes:

(a1) oxidizing the surface of the first silicon film to form a first silicon oxide film;

(a2) forming a first silicon nitride film over the first silicon oxide film;

(a3) oxidizing the surface of the first silicon nitride film to form a second silicon oxide film; and

(a4) forming a third silicon oxide film over the second silicon oxide film to form the first dielectric film comprising the first silicon oxide film, the first silicon nitride film, the second silicon oxide film and the third silicon oxide film.

17 A manufacturing method according to claim 15,

wherein the first conductive film is a stacked film formed by stacking a second silicon film and a refractory

metal silicide film from the lower layer, or a stacked film formed by stacking the second silicon film, a barrier metal film and a refractory metal film from the lower layer.

18. A manufacturing method according to claim 15, comprising the steps of:

(g) forming a semiconductor chip of a planar rectangular shape having the power MISFET; and

(h) wire bonding the semiconductor chip to a mounting substrate by a first wire electrically connecting with the gate of the power MISFET and a second wire electrically connecting with the drain of the power MISFET,

wherein power MISFETs are arranged of four corners of the semiconductor chip, and the first wire and the second wire are arranged such that the first direction along which the first wire extends and the second direction along which the second wire extends are in perpendicular to each other in a plane.

19. A manufacturing method according to claim 15,

wherein the capacitor element and the resistor element form an analog circuit.

20. A manufacturing method according to claim 19,

wherein the power MISFET forms a first circuit for

processing signals in a first frequency band and a second circuit for processing signals in a second frequency band different from the first frequency wave, and the analog circuit selects the first circuit or the second circuit.

21. A semiconductor device in which plural wiring layers are formed over a semiconductor substrate and an active elements and an inductor are formed over the semiconductor substrate,

wherein the inductor is formed to the uppermost wiring layer among the plural wiring layers.

22. A semiconductor device according to claim 21, wherein a bonding pad is formed to the device forming surface of the semiconductor substrate and the bonding pad is formed to the uppermost wiring layer.

23. A semiconductor device according to claim 21, wherein the thickness of the uppermost wiring layer is greater than the thickness of the lower wiring layer formed below the uppermost wiring layer.

24. A semiconductor device according to claim 21, wherein a capacitor element having a lower electrode and an upper electrode is formed over the semiconductor substrate and the

inductor is formed above the upper electrode of the capacitor element.

25. A semiconductor device according to claim 24, wherein the lower electrode and the upper electrode of the capacitor element are formed of a metal film.

26. A semiconductor device according to claim 21, wherein the device has plural stages of circuits operating at a frequency of 800 MHz or higher and the inductor forms an inter-stage matching circuit between the circuits.

27. A semiconductor device according to claim 21, wherein the inductor has first and second terminals, the first terminal is formed in the uppermost wiring layer and the second terminal is formed in the lower wiring layer below the uppermost wiring layer.

28. A semiconductor device in which the first wiring layer and a second wiring layer above the first wiring layer are formed over a semiconductor substrate, and a first capacitor element having a first lower electrode and a first upper electrode, and a second capacitor element having a second lower electrode and a second upper electrode are formed over the semiconductor substrate,

wherein the first lower electrode and the second lower electrode are formed, respectively, to the first wiring layer and the second wiring layer,

wherein a first circuit operating in a first frequency band and a second circuit operating in a second frequency band are formed over the semiconductor substrate,

wherein the first capacitor element is included in the first circuit and the second capacitor element is included in the second circuit, and

wherein the frequency included in the first frequency band is lower than the frequency included in the second frequency band.

29. A semiconductor device according to claim 28, wherein the first frequency band includes 100 MHz and the second frequency band includes 800 MHz to 900 MHz or 1.8 GHz to 1.9 GHz.

30. A semiconductor device according to claim 29, wherein the first lower electrode and the first upper electrode comprise silicon as a main ingredient and the second lower electrode and the second upper electrode comprise a metal as a main ingredient.

31. A semiconductor device according to claim 29, wherein

the second circuit is formed with plural stages of circuits and the second capacitor element forms an inter-stage matching circuit between plural stages of circuits in the second circuit.

32. A semiconductor device comprising, over a semiconductor substrate:

a MISFET formed of source, drain, and gate electrode;

a resistor element;

a first capacitor element formed of a first lower electrode and a first upper electrode;

a second capacitor element formed of a second lower electrode and a second upper electrode; and

an inductor,

wherein a first silicon layer and a second silicon layer disposed over the first silicon layer are formed over the semiconductor substrate,

wherein a first metal layer, a second metal layer disposed over the first metal layer and a third metal layer disposed over the second metal layer are formed over the semiconductor substrate,

wherein the first silicon layer forms the first lower electrode of the first capacitor element and the resistor element,

wherein the second silicon layer forms the first upper

electrode of the first capacitor element and the gate electrode of the MISFET, and

wherein the first metal layer forms the second lower electrode of the second capacitor element, the second metal layer forms the second upper electrode of the second capacitor element, and the third metal layer forms the inductor.

33. A semiconductor device in which a passive element having two terminals is formed over the main surface of a semiconductor substrate, a conductive film is formed to the rear face of the semiconductor substrate, the conductive film is connected with a fixed potential and one of the terminals of the passive element is electrically connected with the conductive film.

34. A semiconductor device according to claim 33, wherein the passive element includes one or more of resistor element, capacitor element, and inductor.

35. A semiconductor device according to claim 33, wherein the fixed potential is a ground potential.

36. A semiconductor device according to claim 33, wherein an impurity layer is formed by introduction of impurities in

the semiconductor substrate and one of the terminals of the passive element and the conductive film are electrically connected by way of the impurity layer.

37. A semiconductor device according to claim 33, wherein a MISFET having gate and drain disposed to the main surface of the semiconductor substrate and a source disposed to the rear face of the semiconductor substrate is formed, and the source of the MISFET is electrically connected with the conductive film.

38. A semiconductor device comprising: a well formed to the main surface of the semiconductor substrate; and a first MISFET having source, drain, and gate disposed in the well over the main surface of the semiconductor substrate,

wherein the conductive film is formed to the rear face of the semiconductor substrate, the conductive film is connected with a fixed potential, and the well is electrically connected with the conductive film.

39. A semiconductor device according to claim 38, wherein a second MISFET having gate and drain disposed to the main surface of the semiconductor substrate and the source disposed to the rear face of the semiconductor substrate is formed, and the source of the second MISFET is electrically

connected with the conductive film.

40. A semiconductor device according to claim 38, wherein the well has a p-conduction type and the fixed potential is a ground potential.

41. A semiconductor device according to claim 38, wherein an impurity layer is formed by introduction of impurities in the semiconductor substrate, and the well and the conductive film are electrically connected by way of the impurity layer.

42. A semiconductor device comprising: a well formed to the main surface of a semiconductor substrate; a first MISFET having, in the well, a source, a drain and a gate disposed to the main surface of the semiconductor substrate; a second MISFET having gate and drain disposed to the main surface of the semiconductor substrate and a source disposed to the rear face of the semiconductor substrate; a passive element formed over the main surface of the semiconductor substrate and having two terminals; and a conductive film formed to the rear face of the semiconductor substrate,

wherein the conductive film is connected with a fixed potential, and one of the terminals of the passive element, the well, and the source of the second MISFET are electrically connected with the connective film.

43. A semiconductor device comprising: a first circuit block and a second circuit block formed over a semiconductor substrate; and a conductive film formed to the rear face of the semiconductor substrate and connected with a ground potential,

wherein the first circuit block and the second circuit block include one of a circuit amplifying high frequency power or a circuit controlling the circuit block amplifying high frequency power, each of the first circuit block and the second circuit block has an impurity layer formed by introduction of impurities, and the first circuit block and the second circuit block are electrically connected by way of the impurity layer with the conductive film.

44. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a first insulation film over a semiconductor substrate;

(b) planarizing the surface of the first insulation film;

(c) forming a first conductive film over the first insulation film and patterning the first conductive film;

(d) forming a second insulation film over the first conductive film and patterning the second insulation film; and

(e) forming a second conductive film over the second insulation film and patterning the second conductive film, thereby forming a second capacitor element having the first conductive film as a lower electrode, the second insulation film as the capacitor dielectric film, and the second conductive film as the upper electrode.

45. A method of manufacturing a semiconductor device according to claim 44, comprising the steps of:

(f) forming a third insulation film over the second conductive film; and

(g) forming a third conductive film over the third insulation film and patterning the third conductive film, thereby forming an inductor.

46. A method of manufacturing a semiconductor device according to claim 45, comprising the steps of: forming the first conductive film and the second conductive film from a metal film; and forming the first capacitor element having the upper electrode and the lower electrode comprising silicon as a main ingredient below the first insulation film.